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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	3

Complete if Known	
Application Number	10/674,085
Filing Date	September 29, 2003
First Named Inventor	Elias Fallon et al.
Group Art Unit	~~Not Yet Assigned~~ 2825
Examiner Name	~~Not Yet Assigned~~ Helen Rossoshek
Attorney Docket Number	2879-030564

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2]	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
HR	1	6,161,078		Ganley	12/12/2000	
HR	2	6,282,694		Cheng et al.	08/28/2001	
HR	3	6,550,046	B1	Balasa et al.	04/15/2003	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published.	T[2]
HR	4	FLORIN BALASA and KOEN LAMPAERT, "Module Placement For Analog Layout Using The Sequence-Pair Representation", Proc. ACM/IEEE Design Automation, pp. 274-279, (June 1999).	
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Examiner Signature	/Helen Rossoshek/	Date Considered	05/04/2006

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Group Art Unit	~~Not Yet Assigned~~ 2825
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HR	14	MARGHERITA PILLAN and DONATELLA SCIUTO, "Constraint Generation And Placement For Automatic Layout Design Of Analog Integrated Circuits", pp. 355-358.	
	15	YINGXIN PANG, FLORIN BALASA, KOEN LAMPAERT and CHUNG-KUAN CHENG, "Block Placement Symmetry Constraints Based On The O-Tree Non-Slicing Representation", Proc. ACM/IEEE Design Automation Conference, pp. 464-467, (June 2000).	
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Examiner Signature	/Helen Rossoshek/	Date Considered	05/04/2006

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HR	24	R. OKUDA, T. SATO, H. ONODERA and K. TAMARU, "An Efficient Algorithm For Layout Compaction Problem With Symmetry Constraints", In Proc. IBBB ICCAD, pp. 148-151, (November 1989).	

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